REMARKS / DISCUSSION OF ISSUES

Claims 1-20 are pending in the application. Claims 7-20 are newly added.

The claims are amended to remove limitations added in the applicants' prior responses. Because these prior responsive have not affected the determination of patentability of the claims, the applicants herein recant and retract any and all remarks in the applicants' prior responses. Claims 1-6 are amended to restore the intended scope of the claims as originally filed.

The Office action rejects claims 1-6 under 35 U.S.C. 103(a) over Hauck et al. (*The Chimaera Reconfigurable Functional Unit*, hereinafter Hauck) and DeHon (*Notes on Coupling Processors with Reconfigurable Logic)*. The applicants respectfully traverse this rejection.

Claim 1, upon which claims 2-4 depend, claims a data processing device that includes input and output units coupled to source and destination registers, a first programmable connection circuit between an unit input and logic blocks, for selectively coupling inputs of the logic blocks to bits from the unit input, dependent on a configured function, and a second programmable connection circuit between the logic blocks and a unit output, for selectively coupling bits of the outputs of the logic blocks to the unit output in a second order of bits, dependent on the configured function.

MPEP 2142 states:

> "To establish a *prima facie* case of obviousness ... the prior art reference (or references when combined) ***must teach or suggest all the claim limitations***... If the examiner does not produce a *prima facie* case, the applicant is under no obligation to submit evidence of nonobviousness."

Both Hauck and DeHon fail to teach a connection circuit between the logic blocks and a unit output, for selectively coupling bits of the outputs of the logic blocks to the unit output in an order of bits that is dependent on a configured function.

The Office action refers to the Office action of 15 September 2004, which asserts that Hauck's output multiplexers connected to outputs O1...O4 correspond to

the applicants' claimed second connection circuit. As taught and claimed by the applicants, the second connection circuit is configured to allow a re-ordering of the output bits of the configurable function unit, to improve the efficiency of the configurable function units. Hauck's output multiplexers do not allow for a re-ordering of the output bits of the configurable function unit, because each logic block, within which the output multiplexers are located, is associated with a single bit of the source/destination registers.

Hauck specifically teaches a bit-slice architecture, wherein the configurable function units are arranged in a row and column configuration. As specifically taught by Hauck, "The reconfigurable logic is broken into rows of logic cells between routing channels. Within that row, there is one cell per bit in the processor's memory word, so for a 32-bit processor there are 32 cells per row. All cells in a given column *i* have access to the *i*th bits of registers R0-R8" (Hauck, page 89, lines 3-8). That is, each of the 4-input, 4-output logic cells of Hauck are assigned to a particular bit-column of Hauck, and the only between-column communication, to route a bit from one column to another, occurs at the routing channels at the input to the logic blocks, and not at the output of the blocks. Some of the advantages of providing a connection circuit at the output of a functional block as well as at its input are noted at page 3, lines 4-17 of the applicants' specification.

Because Hauck's output multiplexers do not allow for a reordering of bits to an output unit that is coupled to a destination register, as specifically claimed in claim 1, the applicants respectfully request the Examiner's reconsideration of the rejection of claims 1-4 under 35 U.S.C. 103(a) over Hauck and DeHon.

In like manner, claim 5 claims a method of programming a configurable processing device that includes programming connection circuits in from and subsequent to programmable logic blocks so as to perform a first routing of bits of an input operand and a second routing of outputs of the programmable logic blocks to bits of the result data word. And, claim 6 claims a method that includes selectively coupling bits of an output word to bits of a result word, dependent on a configured function.

As noted above, Hauck's output multiplexers do not provide a re-routing of bits of an output word, as claimed in each of claims 5 and 6, and the applicants respectfully request the Examiner's reconsideration of the rejection of claims 5 and 6 under 35 U.S.C. 103(a) over Hauck and DeHon.

In view of the foregoing, the applicants respectfully request that the Examiner withdraw the objection(s) and/or rejection(s) of record, allow all the pending claims, and find the application in condition for allowance. If any points remain in issue that may best be resolved through a personal or telephonic interview, the Examiner is respectfully requested to contact the undersigned at the telephone number listed below.

Respectfully submitted,

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